REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claims 1-13 are objected to because of minor informalities that are alleged to be present in the claims.

In response to the formal objections to the claims, applicants have amended Claims 1, 4, 6 and 9 in the manner indicated supra and have cancelled Claims 2 and 3. Specifically, applicants have amended Claim 1 to positively recite that the block emitter polysilicon region comprises at least a polysilicon emitter. Support for this amendment to Claim 1 is found at paragraph [0064] of the originally filed specification. Additionally, applicants have amended Claim 1 to indicate which edge and which direction that the various layers are self-aligned at. Support for this amendment to Claim 1 is found at paragraph [0070] and in FIG. 1H of the present application.

The above amendments to Claim 1 necessitated the amendments to Claims 4 and 6 as well as the cancellation of Claims 2 and 3.

In regard to Claim 9, applicants have amended that claim by changing the term "directed" to "directly", as suggested by the Examiner in the present Office Action.

In the present Office Action, the Examiner avers that Claim 7 recites subject matter that is not all readable on the elected species of FIGS. 2A-2H. Applicants acknowledge this and submit that the subject matter related to the wide spacer reads on the elected species; the other subject matter recited in Claim 7, i.e., double spacers and L-shaped spacer do not read on the elected species. Applicants have not amended Claim 7 at the present time since they believe that the subject matter of Claim 7 that is not readable on the elected species will be rejoined with the

species elected in this application. In the event that this rejoinder can not occur, applicants will cancel the non-readable subject matter from Claim 7, if so requested in a subsequent Action.

Based on the above amendments and remarks, the objections to the claims raised in the present Office Action have been obviated. Reconsideration and withdrawal of the objections to the claims are thus respectfully requested.

Claims 1-11 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,767,798 to Kalnitsky, et al. ("Kalnitsky, et al."). Claims 12 and 13 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of Kalnitsky, et al. and U.S. Patent No. 6,399,993 to Ohnishi, et al. ("Ohnishi, et al.").

Concerning the §102(e) rejection, it is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants submit that the claims of the present application are not anticipated by the disclosure of Kalnitsky, et al. since the applied reference does not disclose applicants' claimed structure. Specifically, Kalnitsky, et al. do not disclose a bipolar transistor which includes, among other features, a first silicide layer located on a raised extrinsic base region where the first silicide layer has an inner vertical edge that is self-aligned to a vertical sidewall of a block polysilicon emitter region and a second silicide layer located on a polysilicon emitter and within

the block polysilicon emitter region, said second silicide layer having an outer edge that is self-aligned to the inner vertical edge of the first silicide layer, as is recited in Claim 1 of the present application.

Kalnitsky, et al. provide a bipolar transistor that has a raised extrinsic base such that the link base resistance is reduced by providing an extrinsic base which is thicker than the intrinsic base. Applicants observe that FIG. 2 and FIG. 3H shows the final bipolar transistor structure of the prior art reference. In those figures, reference numeral 52 or 154 denotes the silicide that is present in the structure. Applicants observe that the silicide 52 or 154 located atop the extrinsic base region layer 24 or 144 does not have an inner vertical edge that is self-aligned to a vertical sidewall of a block polysilicon emitter region. Instead, the silicide 52 or 154 located atop the extrinisic base 24 or 144 has an inner vertical edge that is aligned to a bottom edge of a spacer. Applicants further observe that the silicide 52 or 154 atop the emitter does not have an outer edge that is self-aligned to the inner vertical edge of the silicide atop the extrinsic base.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Kalnitsky, et al. Applicants respectfully submit that the instant §102 rejection has been obviated and withdrawal thereof is respectfully requested.

With respect to the §103 rejection, applicants submit that the claims of the present invention are not rendered unpatentable by the combined disclosures of Kalnitsky, et al. and Ohnishi, et al. since none of the applied references teach or suggest applicants' claimed structure.

The principle reference spurring the obviousness rejection, i.e., Kalnitsky, et al., is defective for the same reasons as discussed above under the anticipation rejection. Applicants

thus incorporate the above remarks made under the anticipation rejection herein by reference. To reiterate: Kalnitsky, et al. do not teach or suggest a bipolar transistor that includes, among other features, a first silicide layer located on a raised extrinsic base region where the first silicide layer has an inner vertical edge that is self-aligned to a vertical sidewall of a block polysilicon emitter region and a second silicide layer located on a polysilicon emitter and within the block polysilicon emitter region, said second silicide layer having an outer edge that is self-aligned to the inner vertical edge of the first silicide layer, as is recited in Claim 1 of the present application.

Kalnitsky, et al. provide a bipolar transistor that has a raised extrinsic base such that the link base resistance is reduced by providing an extrinsic base which is thicker than the intrinsic base. Applicants observe that FIGs. 2 and 3H shows the final bipolar transistor structure of the prior art reference. In those figures, reference numeral 52 or 154 denotes the silicide that is present in the structure. Applicants observe that the silicide 52 or 154 located atop the extrinsic base region layer 24 or 144 does not have an inner vertical edge that is self-aligned to a vertical sidewall of a block polysilicon emitter region. Instead, the silicide 52 or 154 located atop the extrinisic base 24 or 144 has an inner vertical edge that is aligned to a bottom edge of a spacer. Applicants further observe that the silicide 24 or 154 atop the emitter does not have an outer edge that is self-aligned to the inner vertical edge of the silicide atop the extrinsic base.

The above defects in the principle reference are not alleviated by Ohnishi, et al. since the applied secondary reference also does not teach or suggest the features mentioned above. That is, Ohnishi, et al. do not teach or suggest a bipolar transistor which includes, among other features, a first silicide layer located on a raised extrinsic base region where the first silicide layer has an inner vertical edge that is self-aligned to a vertical sidewall of a block polysilicon

emitter region and a second silicide layer located on a polysilicon emitter and within the block polysilicon emitter region, said second silicide layer having an outer edge that is self-aligned to the inner vertical edge of the first silicide layer, as is recited in Claim 1 of the present application.

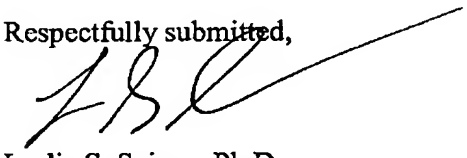
Ohnishi, et al. provide a bipolar transistor that includes a base layer 20a of SiGe single crystals and an emitter layer 26 of almost 100% Si single crystals stacked over a collector diffused layer 9. Applicants observe that FIGs. 15B, 16 and 18 shows the final bipolar transistor structure of the prior art reference. In that figure, reference numeral 27 denotes the silicide that is present in the structure. Applicants observe that the silicide 27 located atop the subcollector 4 (not a base region, as presently claimed) does not have an inner vertical edge that is self-aligned to a vertical sidewall of a block polysilicon emitter region. Instead, that silicide has an inner vertical edge that is aligned to the edge of insulating layer 5a. Applicants further observe that the silicide 27 atop the emitter 21 does not have an outer edge that is self-aligned to the inner vertical edge of the silicide 27 located atop the sub-collector 4.

The §103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed structure to include the various elements recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Leslie S. Szivos, Ph.D
Registration No. 39,394

SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza, Ste. 300
Garden City, New York 11530
(516) 742-4343
Customer No. 23389
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